TC3405

16-Bit, Low Cost, Low Power Sigma-Delta A/D Converter

Features

- 16-bit Resolution at Eight Conversions Per Second, Adjustable Down to 10-bit Resolution at 512 Conversions Per Second
- 1.8V – 5.5V Operation, Low Power Operating 250µA; Sleep: 35µA
- microPort™ Serial Bus Requires only two Interface Lines
- Uses Internal or External Reference
- Automatically Enters Sleep Mode when not in use
- One Differential and Three Single-ended Inputs with Built-In Multiplexer
- V_{DD} Monitor and Reset Generator Operational in Shutdown Mode

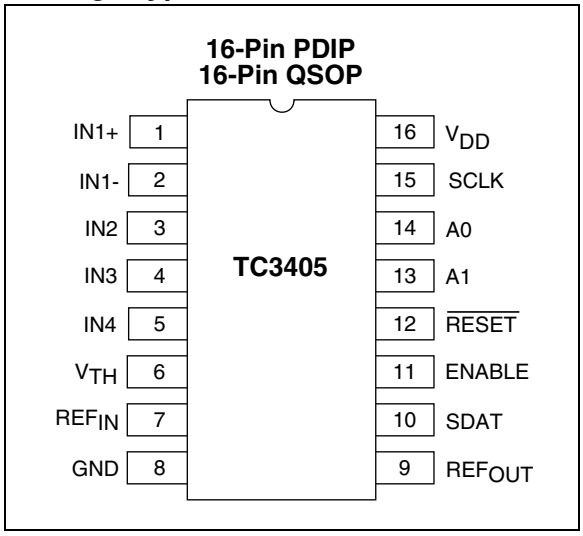
Applications

- Consumer Electronics, Thermostats, CO Monitors, Humidity Meters, Security Sensors
- Embedded Systems, Data Loggers, Portable Equipment
- Medical Instruments

Device Selection Table

Part Number	Package	Temperature Range
TC3405VPE	16-Pin PDIP (Narrow)	0°C to +85°C
TC3405VQR	16-Pin QSOP Narrow)	0°C to +85°C

Package Type



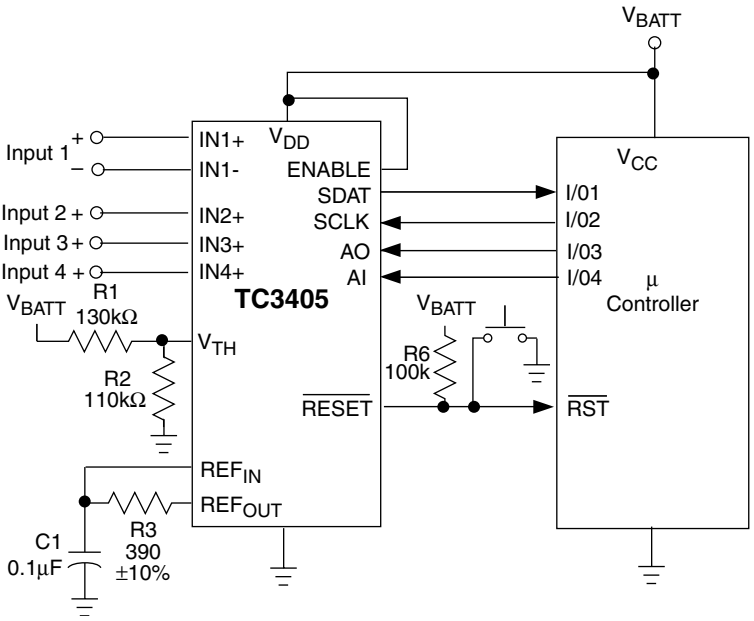
General Description

The TC3405 is a low cost, low power analog-to-digital converter based on Microchip's Sigma-Delta technology. It will perform 16-bit conversions (15-bit plus sign) at up to eight per second. The TC3405 is optimized for use as a microcontroller peripheral in low cost, battery operated systems. A voltage reference is included, or an external reference can be used. A V_{DD} monitor with a reset generator provides Power-on Reset and Brown-out protection while an extra threshold detector is suitable for use as an early warning power fail detector, or as a Wake-up Timer.

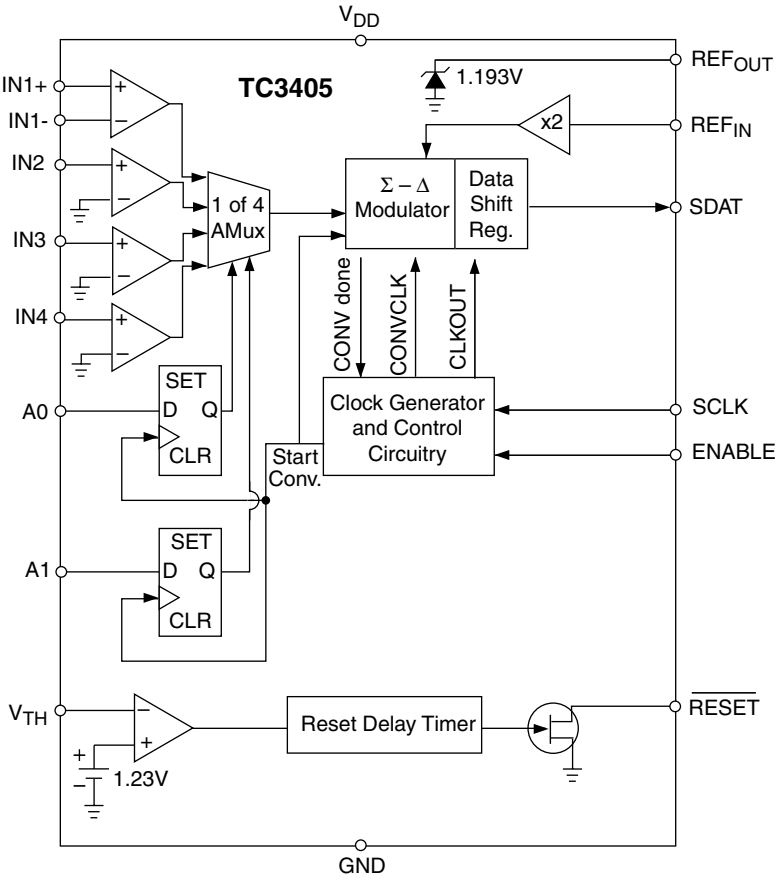
The TC3405's 2-wire microPort™ digital interface is used for starting conversions and for reading out the data. Driving the SCLK line low starts a conversion. After the conversion starts, each additional falling edge (up to six) detected on SCLK for t_4 seconds reduces the A/D resolution by one bit and cuts conversion time in half. After a conversion is completed, clocking the SCLK line puts the MSB through LSB of the resulting data word onto the SDAT line, much like a shift register. The part automatically sleeps when not performing a data conversion.

The TC3405 is available in a 16-Pin PDIP and a 16-Pin QSOP package.

Typical Application



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Supply Voltage 6.0V
Voltage on Pin:
$\overline{\text{RESET}}$ ..... (GND – 0.3V) to 5.5V
Input Voltage (All Other Pins):
..... (GND – 0.3V) to (V_{DD} + 0.3V)
Operating Temperature Range ..... 0°C to 85°C
Storage Temperature ..... -65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TC3405 DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: T_A = 25°C and V_{DD} = 2.7V, unless otherwise specified. **Boldface** type specifications apply for temperatures of 0°C to 85°C. V_{REF} = 1.25V, Internal Clock Frequency = 520kHz.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Power Supply						
V_{DD}	Supply Voltage	1.8	—	5.5	V	
I_{DD}	Supply Current, During Data Conversion	—	250	—	µA	
$I_{DDSLEEP}$	Supply Current, Sleep Mode	—	35	80	µA	T_A = +25°C
		—	**38**	**50**	µA	
Accuracy (Differential Inputs)						
RES	Resolution	—	16	—	Bits	
INL	Integral Non-Linearity	—	.0038	—	%FSR	V_{DD} = 2.7V
V_{OS}	Offset Error	—	—	**±0.9**	%FSR	IN+, IN- = 0V
V_{NOISE}	Referred to input	—	60	—	µVrms	
CMR	Common Mode Rejection	—	75	—	dB	At DC
FSE	Full Scale Error	—	0.4%	—	%FS	
PSRR	Power Supply Rejection Ratio	—	75	—	dB	V_{DD} = 2.5V to 3.5V
INn+, INn-, INn						
V_{IN}±	Differential Input Voltage	—	—	V_{DD}	V	**Note 1**
	Absolute Voltage Range on INn+, INn-, INn	GND	—	V_{DD}	V	
	Input Bias Current	—	1	100	nA	
C_{IN}	Input Sampling Capacitance	—	2	—	pF	
R_{IN}	Differential Input Resistance	—	2.0	—	MΩ	**Note 2**
REF_{IN}, REF_{OUT}						
V_{REF}	REF_{IN} Voltage Range	0	—	1.25	V	
I_{REF}	REF_{IN} Input Current	—	1	—	µA	
V_{REFOUT}	REF_{OUT} Voltage	1.175	1.193	—	V	
REF_{SINK}	REF_{OUT} Current Sink Capability	—	10	—	µA	
REF_{SRC}	REF_{OUT} Current Source Capability	300	—	—	µA	

Note 1: Differential input voltage defined as (V_{IN}+ – V_{IN}-).
2: Resistance from INn+ to INn- or INn to GND.
3: @ V_{DD} = 1.8V, $I_{SOURCE} \leq 200\mu A$.

TC3405 DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: T_A = 25°C and V_{DD} = 2.7V, unless otherwise specified. **Boldface** type specifications apply for temperatures of 0°C to 85°C. V_{REF} = 1.25V, Internal Clock Frequency = 520kHz.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
SCLK, A0 A1, ENABLE						
V_{IL}	Input Low Voltage	—	—	**0.3 x V_{DD}**	V	
V_{IH}	Input High Voltage	**0.7 x V_{DD}**	—	—	V	
I_{LEAK}	Leakage Current	—	1	—	µA	
SDAT, $\overline{\text{RESET}}$						
V_{OL}	Output Low Voltage	—	—	0.4	V	I_{OL} = 1.5mA
V_{OH}	Output High Voltage (SDAT)	0.9 x V_{DD}	—	—	V	I_{SOURCE} = 400µA **(Note 3)**
V_{DDMIN}	Minimum V_{DD} for $\overline{\text{PFO}}$, $\overline{\text{RESET}}$ Valid	—	1.1	1.3	µA	
V_{TH}, PFI						
V_{CCPFI}	PFI Input Voltage Range	0	—	V_{DD}	V	
	V_{TH}, PFI Input Current	-0.1	.01	0.1	µA	
V_{THR}	Threshold (V_{TH}, PFI)	—	1.23	—	V	
	Threshold Hysteresis	—	30	—	mV	
	Threshold Tempco	—	30	—	ppm/°C	

Note 1: Differential input voltage defined as (V_{IN}+ – V_{IN}-).
2: Resistance from INn+ to INn- or INn to GND.
3: @ V_{DD} = 1.8V, $I_{SOURCE} \leq$ 200µA.

TC3405 AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: T_A = 25°C and V_{DD} = 2.7V, unless otherwise specified. **Boldface** type specifications apply for temperatures of 0°C to 85°C. V_{REF} = 1.25V, Internal Clock Frequency = 520kHz.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_1	Resolution Reduction Clock Width	1	—	—	µsec	Width of SCLK (Negative)
t_2	Resolution Reduction Clock Width	1	—	—	µsec	Width of SCLK (Positive)
t_3	Conversion Time (15-bit Plus Sign)	—	125	—	msec	16-bit Conversion, T_A = 25°C **(Note 1)**
	Conversion Time (14-bit Plus Sign)	—	t_3/2.0	—	msec	15-bit Conversion
	Conversion Time (13-bit Plus Sign)	—	t_3/4.0	—	msec	14-bit Conversion
	Conversion Time (12-bit Plus Sign)	—	t_3/7.8	—	msec	13-bit Conversion
	Conversion Time (11-bit Plus Sign)	—	t_3/15.1	—	msec	12-bit Conversion
	Conversion Time (10-bit Plus Sign)	—	t_3/28.6	—	msec	11-bit Conversion
	Conversion Time (9-bit Plus Sign)	—	t_3/51.4	—	msec	10-bit Conversion
t_4	Resolution Reduction Window	—	t_3/85.7	—	msec	Width of SCLK
t_5	SCLK to Data Valid	**1000**	—	—	nsec	SCLK Falling Edge to SDAT Valid
t_6	Address Setup	**0**	—	—	nsec	Address Valid to SCLK
t_7	Address Hold	**1000**	—	—	nsec	SCLK to Address Valid Hold
t_8	Acknowledge Delay	—	—	**1000**	nsec	SCLK to SDAT Delay
t_9	$\overline{\text{RESET}}$ Active Time-out Period	—	t_3*2	—	msec	Delay from POR or Brown-out Recovery to $\overline{\text{RESET}}$ = V_{OH}
t_{11}	$\overline{\text{RESET}}$ Delay	5	—	**64**	µsec	Delay V_{TH} Falling at 10V/msec to $\overline{\text{RESET}}$ Low

Note 1: Nominal temperature drift is -2830ppm/C° for temperature less than 25°C and -1340ppm/°C for temperatures greater than 25°C.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin No. (16-Pin PDIP) (16-Pin QSOP)	Symbol	Description
1	IN1+	Analog Input. This is the positive terminal of a true differential input consisting of IN1+ and IN1-. V_{IN1} = (IN1+ – IN-). See Section 1.0, Electrical Characteristics.
2	IN1-	Analog Input. This is the negative terminal of a true differential input consisting of IN1+ and IN1-. V_{IN1} = (IN+ – IN-) IN1- can swing to, but not below, ground. See Section 1.0, Electrical Characteristics.
3	IN2	Analog Input. This is the positive terminal of a true differential input with the negative input tied internally to GND. See Section 1.0, Electrical Characteristics.
4	IN3	Analog Input. This is the positive terminal of a true differential input with the negative input tied internally to GND. See Section 1.0, Electrical Characteristics.
5	IN4	Analog Input. This is the positive terminal of a true differential input with the negative input tied internally to GND. See Section 1.0, Electrical Characteristics.
6	V_{TH}	Analog Input. This is the positive input to the internal comparator used to monitor the voltage supply. The negative input is tied to an internal reference. When V_{TH} falls below the internal reference, the reset generator drives $\overline{RESET}$ low. See Section 1.0, Electrical Characteristics.
7	REF_{IN}	Analog Input. The converter's reference voltage is the differential between this pin and ground times two. It may be tied directly to REF_{OUT} or scaled using a resistor divider. Any user supplied reference voltage less than 1.25 may be used in place of REF_{OUT}.
8	GND	Ground Terminal.
9	REF_{OUT}	Analog Output. The internal reference connects to this pin. It may be scaled externally, and tied to the REF_{IN} input to provide the converter's reference voltage. Care must be taken in connecting external circuitry to this pin. This pin is in a high impedance state during Sleep mode.
10	SDAT	Digital Output (push-pull). This is the microPort™ serial data output. SDAT is driven low while the TC3405 is converting data, effectively providing a "busy" signal. After the conversion is complete, every high to low transition on the SCLK pin puts a bit from the resulting data word on the SDAT pin (from MSB to LSB).
11	ENABLE	Digital Input. When this input control is pulled low, the part is internally restarted. That is, any data conversion or data read sequence is cleared and the part goes into Sleep mode. When ENABLE returns high, the part resumes normal operation.
12	$\overline{RESET}$	Digital Output (open drain). This is the output of the V_{DD} monitor reset generator. $\overline{RESET}$ is driven low when a Power-on Reset or Brown-out condition is detected. See Section 1.0, AC Electrical Characteristics.
13	A1	Digital Input. Controls analog multiplexer in conjunction with A0 to select one of the four input channels. This address is latched at the falling edge of the SCLK, which starts an A/D conversion. A1, A0 = 00 = Input 1; 01 = Input 2; 10 = Input 3; 11 = Input 4.
14	A0	Digital Input. Controls analog multiplexer in conjunction with A1 to select one of the four input channels. This address is latched at the falling edge of the SCLK, which starts an A/D conversion. A1, A0 = 00 = Input 1; 01 = Input 2; 10 = Input 3; 11 = Input 4.
15	SCLK	Digital Input. This is the microPort™ serial clock input. The TC3405 comes out of Sleep mode and a conversion cycle begins when this pin is driven low. After the conversion starts, each additional falling edge (up to six) detected on SCLK for t_4 seconds, reduces the A/D resolution by one bit. When the conversion is complete, the data word can be shifted out on the SDAT pin by clocking the SCLK pin.
16	V_{DD}	Power Supply Input.

3.0 DETAILED DESCRIPTION

The TC3405 has a 16-bit sigma-delta A/D converter. It has one differential input, three single-ended inputs, an analog multiplexer and a V_{DD} monitor with reset generator. See the Typical Application circuit and the Functional Block diagram. The key components of the TC3405 are described below.

Also refer to Figure 3-5, A/D Operational Flowchart and the Timing Diagrams, Figure 3-1, Figure 3-2 and Figure 3-3.

3.1 A/D Converter Operation

When the TC3405 is not converting, it is in Sleep mode with both the SCLK and SDAT lines high. An A/D conversion is initiated by a high to low transition on the SCLK line at which time the internal clock of the TC3405 is started and the address value (A0 and A1) is internally latched. The address value steers the analog multiplexer to select the input channel to be converted. Each additional high to low transition of SCLK (following the initial SCLK falling edge) during the time interval t_4, will decrement the conversion resolution by one bit and reduce the conversion time by one half. The time interval t_4 is referred to as the resolution reduction window. The minimum conversion resolution is 10-bits so any more than 6 SCLK transitions during t_4 will be ignored.

After each high to low transition of SCLK, in the t_4 interval, the SDAT output is driven high by the TC3405 to acknowledge that the resolution has been decremented. When the SCLK returns high or the t_4 interval ends, the SDAT line returns low (see Figure 3-2). When the conversion is complete SDAT is driven high. The TC3405 now enters Sleep mode and the conversion value can be read as a serial data word on the SDAT line.

3.2 Reading the Data Word

After the conversion is complete and SDAT goes high, the conversion value can be clocked serially onto the SDAT line by high to low transitions of the SCLK. The data word is in two's compliment format with the sign bit clocked onto the SDAT line, first followed by the MSB and ending in the LSB. For a 16-bit conversion the data word would consist of a sign bit followed by 15 magnitude bits, Table 3-1 shows the data word versus input voltage for a 16-bit conversion. Note that the full scale input voltage range is ±(2 REF_{IN} – 1LSB). When REF_{OUT} is fed back directly to REF_{IN}, an LSB is 73µV for a 16-bit conversion, as REF_{OUT} is typically 1.193V.

Figure 3-4 shows typical SCLK and SDAT waveforms for 16, 12 and 10-bit conversions. Note that any complete convert and read cycle requires 17 negative edge clock pulses. The first is the convert command. Then, up to six of these can occur in the resolution reduction window, t_4, to decrement resolution. The remaining pulses clock out the conversion data word.

TABLE 3-1: DATA CONVERSION WORD VS. VOLTAGE INPUT (REF_{IN} = 1.193V)

Data Word	INn+ – INn- (Volts)
0111 1111 1111 1111	2.38596 (Positive Full Scale)
0000 0000 0000 0001	72.8 E -6
0000 0000 0000 0000	0
1111 1111 1111 1111	-72.8 E -6
1000 0000 0000 0001	-2.38596 (Negative Full Scale)
1000 0000 0000 0000	Reserved Code

The SCLK input has a filter which rejects any positive or negative pulse of width less than 50nsec to reduce noise. The rejection width of this pulse can vary between 50nsec and 750nsec depending on processing parameters and supply voltage.

Figure 3-1 and Table 3-2 show information for determining the mode of operation for the TC3401 part by recording the value of SDAT for SCLK in a high, then low, then high state. For example, if SCLK goes through a 1-0-1 transition and the corresponding values of SDAT are 1-1-0, then the SCLK falling edge started a new data conversion. A 0-1-0 for SDAT would have indicated a resolution reduction had occurred. This is useful if the microcontroller has a Watchdog Reset or otherwise loses track of where the TC3405 is in the conversion and data readout sequence. The microcontroller can simply transition SCLK until it "finds" a Start Conversion condition.

FIGURE 3-1: SCLK, SDAT LOGIC STATE DIAGRAM

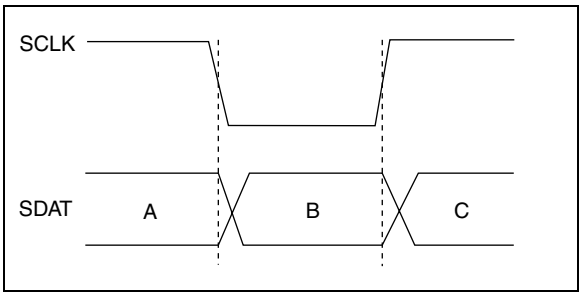


TABLE 3-2: SCLK, SDAT LOGIC STATE

A	B	C	Status
1	1	0	Start Conversion
0	1	0	Resolution Reduction
x	1	1	Data Transfer
x	0	0	Data Transfer or Busy*

***Note:** The code X00 has a dual meaning: Data Transfer or Busy converting. To avoid confusion, the user should send only the required number of pulses for the desired resolution, then wait for SDAT to rise to 1, indicating conversion is complete before clocking SCLK again to read out data bits.

FIGURE 3-2: CONVERSION AND DATA OUTPUT TIMING

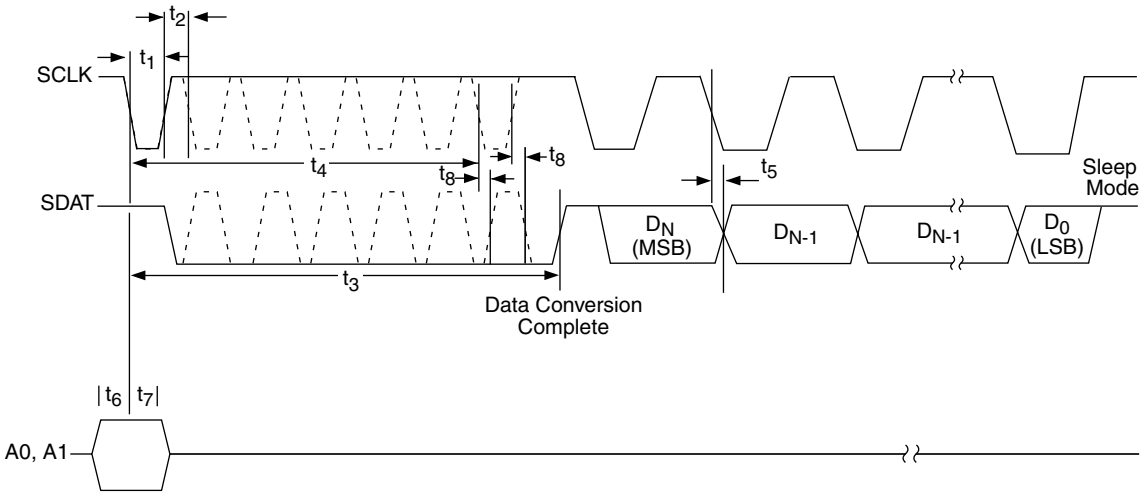


FIGURE 3-3: RESET AND POWER FAIL TIMING

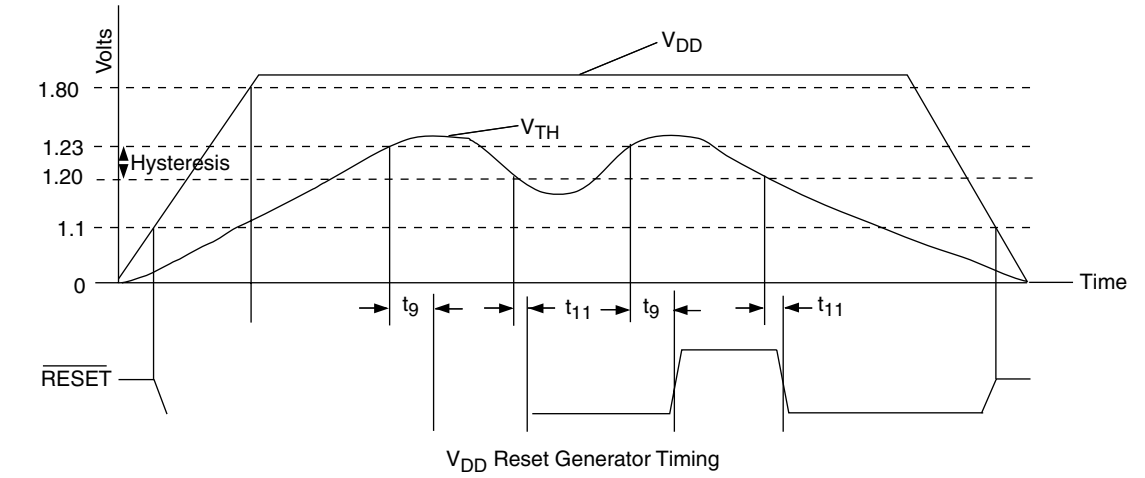


FIGURE 3-4: SCLK AND SDAT WAVEFORMS FOR 16, 12 AND 10-BIT CONVERSIONS

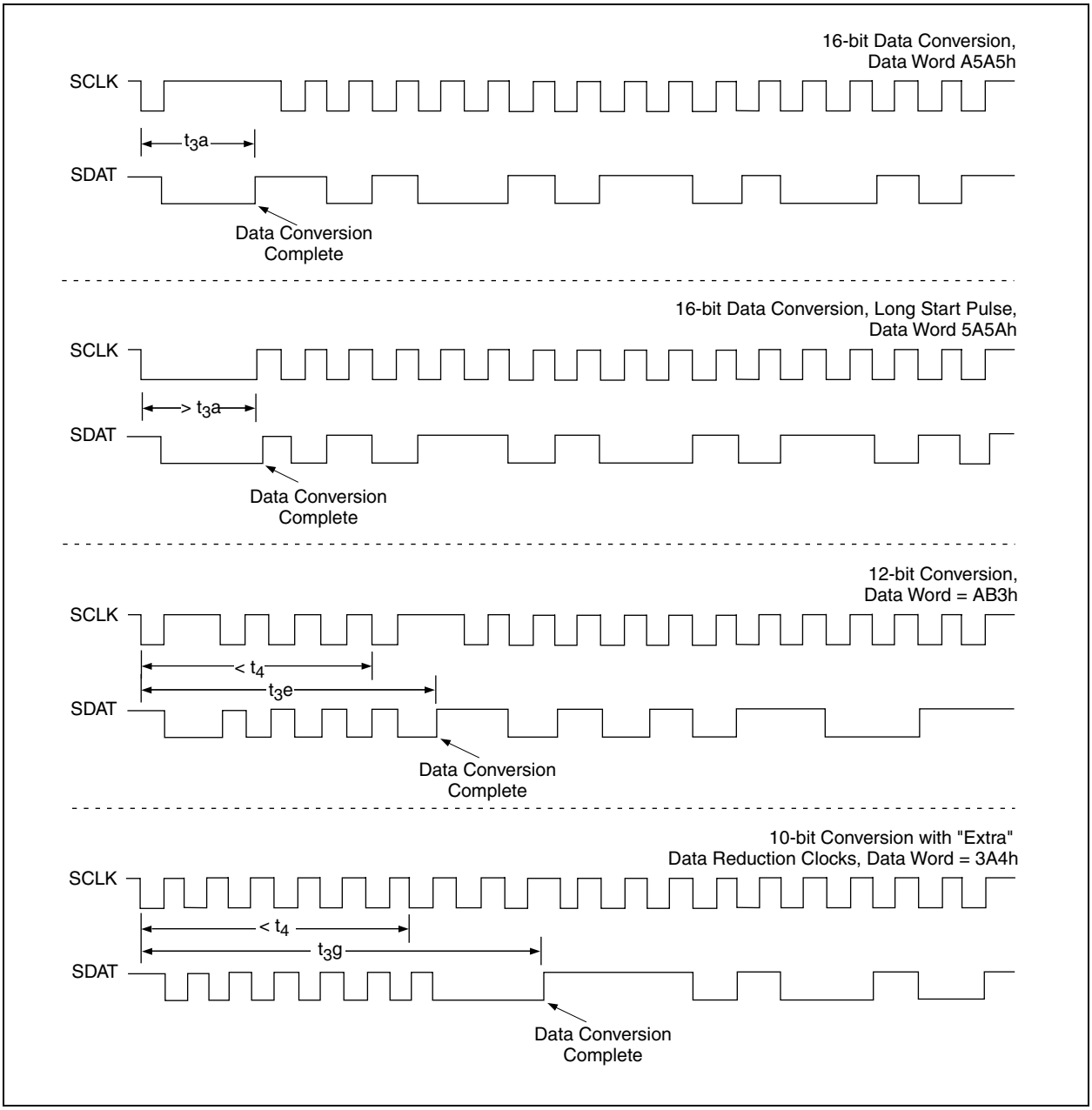
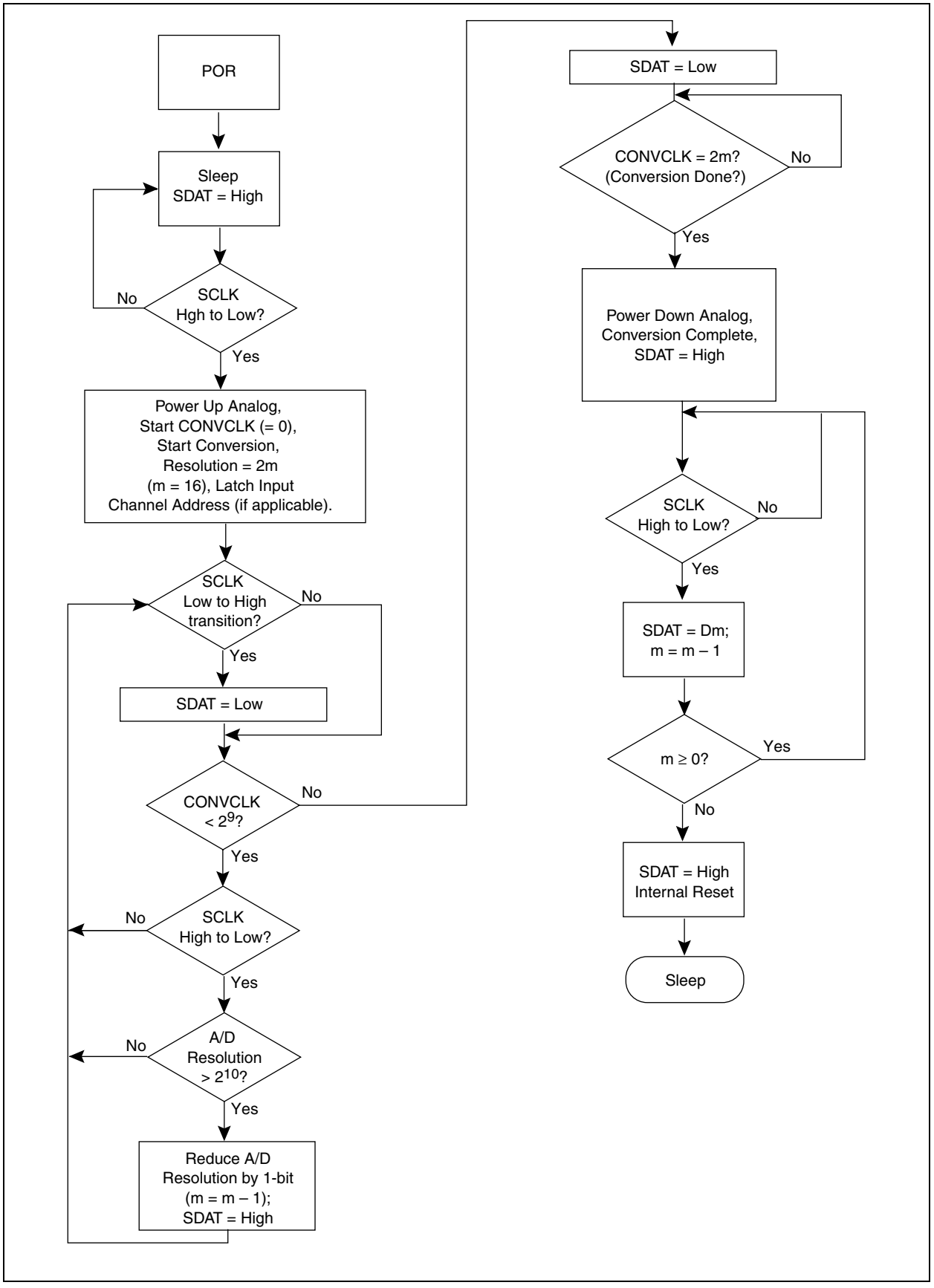


FIGURE 3-5: A/D OPERATIONAL FLOWCHART



3.3 V_{DD} Monitor

The TC3405 $\overline{\text{RESET}}$ output is in high impedance provided the voltage at V_{TH} is greater than the internal voltage reference. This reference is approximately the same value as the voltage appearing at REF_{OUT}. When V_{TH} is less than the internal reference, $\overline{\text{RESET}}$ is pulled low. When V_{TH} rises above the internal reference voltage again, $\overline{\text{RESET}}$ is held low for the reset active time-out period, t_g, before being released. The $\overline{\text{RESET}}$ output is valid for V_{DD} = 1.3V to 5.5V.

When used to generate a Power-on or Brown-out Reset, an external resistor network is required to divide the appropriate V_{DD} threshold down to 1.23V at the V_{TH} input, (See the Typical Application circuit). For example, to generate a POR for a V_{DD} at 3V -10%, the values of R1 and R2 should be 137kΩ and 115kΩ respectively.

Since $\overline{\text{RESET}}$ is an open drain, it can be wired-OR'ed with another open drain or external switch if desired.

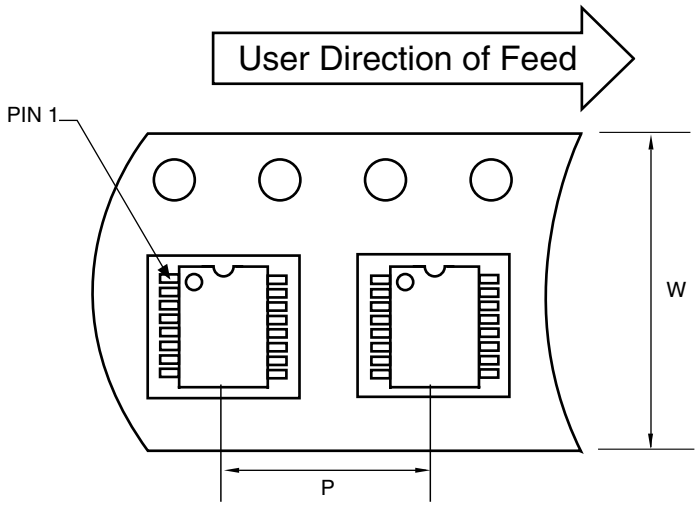
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

Package marking data not available at this time.

4.2 Taping Forms

Component Taping Orientation for 16-Pin QSOP (Narrow) Devices



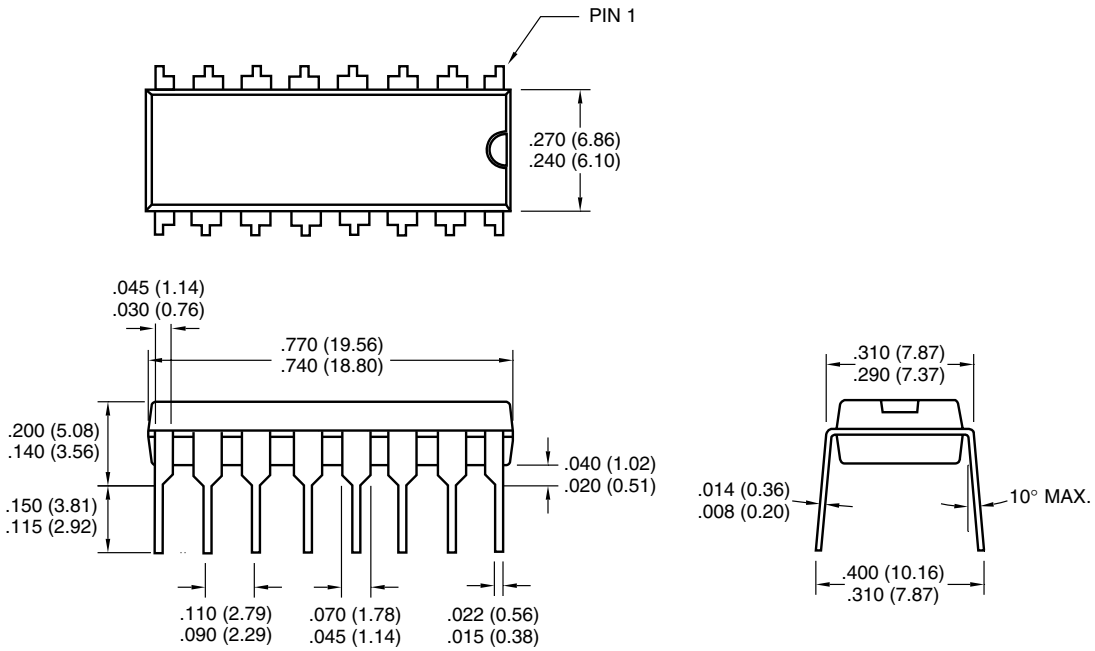
Standard Reel Component Orientation
for TR Suffix Device

Carrier Tape, Reel Size, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
16-Pin QSOP (N)	12 mm	8 mm	2500	13 in

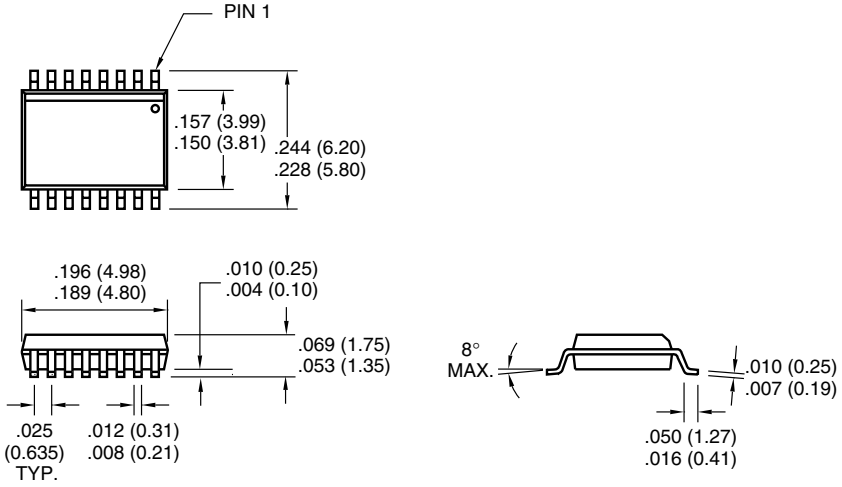
4.3 Package Dimensions

16-Pin PDIP (Narrow)



Dimensions: inches (mm)

16-Pin QSOP (Narrow)



Dimensions: inches (mm)

SALES AND SUPPORT

Data Sheets
Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

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2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
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Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

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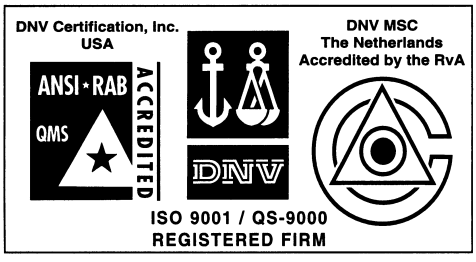

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